EE4350 Final Project

Spring 2025 – 6 Bit DAC Design

Description

You were recently hired as an Analog Mixed Signal Designer at Ames Silicon Solutions, Inc. Currently, your company is working on designing an ASIC (Application Specific Integrated Circuit) for monitoring soil conditions in the area. One of the components needed in this ASIC is a DAC (Digital to Analog Converter).

The system architect has determined that, for the best cost-performance tradeoff, the DAC should be a low-resolution DAC with high linearity. Your company already has many DAC designs but none of them meet the needs of this ASIC so she requested that your team design a new DAC.

Your manager performed some initial analysis and has determined the best architecture to meet the specifications given by the system architect. He has tasked you to design, layout, and verify the DAC as well as any support circuitry needed before the tapeout deadline.

DAC Architecture

The DAC should have the following characteristics:

- Resolution = 6 bits
- 12 pins comprised of 6 digital inputs, 2 supply inputs, one V_{REF} input, and 2 analog outputs (See Figure 1) in addition to GND.
    - Digital inputs defined by $V_H=V_{DD}$ and $V_L=GND$
    - The outputs are referenced to GND
    - V_{OUT} is the output voltage corresponding to the binary input
    - V_{OUT} bar is the output voltage corresponding to the complement of the binary input
- Either an R2R or a current steering architecture is to be used
    - If selecting the current steering DAC architecture, the output due to the 3 least-significant bits should be binary weighted and the output due to the 3 most-significant bits be thermometer coded
    - If using the R2R structure, it must operate in the "current-steering mode"
    - In either case the output currents should drive the null port node of an on-chip transresistance amplifier shown in Figure 2 below.

- In either case, the core DAC structure should have a current output that is converted to an output voltage using an on-chip op amp and an on-chip feedback resistor

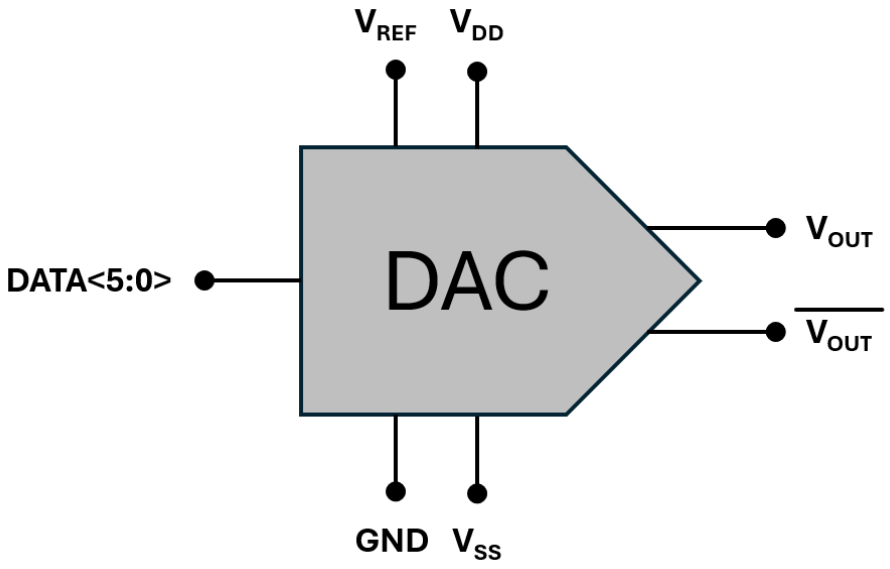

Figure 1 – DAC Diagram

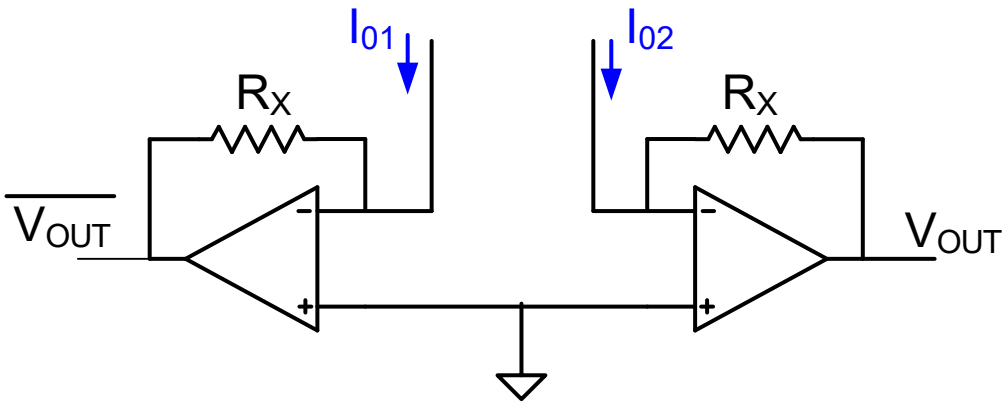

Figure 2 – Transresistance Differential Output Stage

System Specifications

DAC Performance Requirements

You must design the DAC to meet the following specifications:

- ENOB (Effective Number of Bits) from an INL (Integral Non-Linearity) viewpoint ≥ 8 bits

- 90% yield in a 200 point Monte Carlo simulation (180 points meet the ENOB spec)

Other DAC Requirements

Your design must also meet these requirements:

- Entire DAC is designed using components from the “tsmc018rf” PDK
    - The inputs, supplies, and output loading to the DAC in Figure 1 are provided from ideal components – you must design everything inside the DAC with PDK components
- The circuit elements for the 3 most-significant bits must be laid out using the common-centroid technique
    - No common-centroid requirement for the 3 LSB bits
- No bondpads or ESD protection is required
    - This design is made to go in an ASIC so it does not need to interface with the external world

Verification and Reporting Requirements

The following performance should be simulated and reported:

- INL*
- DNL*
- ENOB*
- Offset error*
- Gain error*
- Yield as a percentage from 200 MC runs*
- Quiescent power consumption
- Area (maximum dimensions in µm or mm e.g. 200µm x 300µm)

*typical, mean from MC, standard deviation from MC, and max from MC (MC = Monte Carlo)

Extra Credit: Extract the parasitics from your layout using Calibre PEX, simulate the DAC using the extracted view, and report the performance

Other Assignment Details

- Students may work as individuals or in pairs

- Deliverables will be a final presentation, a final report, and possibly weekly updates
    - Final report forms your tapeout submission
    - Final presentation will be in a design review format
- Design reviews (Final presentations) will be held during prep week at the normal lab time
- Final report will be due Friday at 11:59PM on prep week

Please direct any questions regarding the requirements, deliverables, or design to either the TA or to Dr. Geiger.